following the strategy $C$ are sufficient to guarantee a considerable reduction in the error of the phase estimates of an AR ($p$) process.

(*b*) *Results: part II:* As an example, an AR (4) process is chosen with parameters $a_0 = 1$, $a_1 = 0{\cdot}8$, $a_2 = 0{\cdot}7$, $a_3 = -0{\cdot}2$, and $a_4 = -0{\cdot}1$. Setting the maximum error in any cumulant to be 20% (i.e. $v = 0{\cdot}2$), 10 different sets of the third order cumulants $C_3(m, n)$ are obtained. For each of these 10 sets of cumulants, phases are estimated using the diagonal slice with eqn. 2*b*. The resulting 10 sets of phase estimates are displayed in Fig. 1*a*. For each of the same sets of cumulants, phase estimates are obtained from eqn. 3*b* with 21 TOR equations following strategy $C$. These new sets of phase estimates are plotted in Fig. 1*b*. It is clear that estimates in Fig. 1*b* are much less variable than those in Fig. 1*a*.

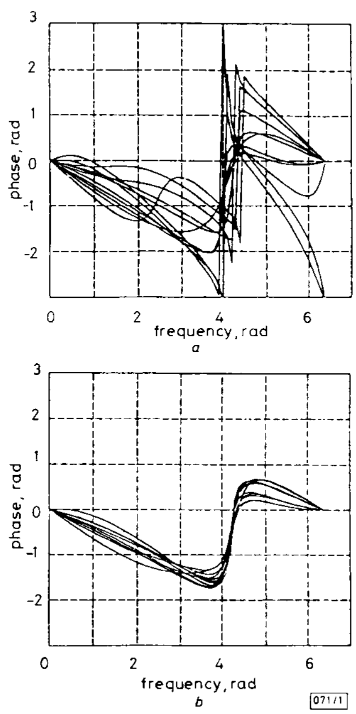


**Fig. 1** *Reconstructed phase against frequency from 10 different realisations of same* AR (*4*) *process*

*a* Reconstruction method based on eqn. 2*b*
*b* Proposed reconstruction method based on eqn. 3*b*

*Summary:* A new algorithm based on eqn. 3*b* has been proposed to estimate the phase of an AR filter. Although the algorithm based on eqn. 2*b* is computationally efficient the proposed algorithm in this Letter provides much less variable and more consistent phase estimates than the algorithm based on eqn. 2*b*.

*20th May 1992*

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## NOVEL APPROACH TO DESIGNING DIGITAL DIFFERENTIATORS

M. A. Al-Alaoui

*Indexing terms: Digital circuits, Circuit design*

A novel approach to designing recursive stable digital differentiators is introduced. A four-step design procedure is presented. The procedure consists of obtaining or designing an integrator and then modifying its transfer function appropriately to obtain a stable differentiator. As an example a second order recursive differentiator is developed.

*Introduction:* Differentiators are useful in the processing of signals in various fields, such as digital control [1], digital image processing [2], communications [3] and biomedical applications [4].

In this Letter, a new approach to designing digital differentiators is introduced. The approach is an extension of the one used in designing analogue differentiators by using integrators. As an example, a novel differentiator is introduced whose magnitude goes to zero at high frequencies. The proposed differentiator is a second-order recursive differentiator. The low order of the differentiator makes it suitable for real-time applications. The accuracy of the proposed differentiator is comparable to that obtained by higher order filters.

*Basic concept:* In analogue signal processing, differentiators are often obtained by inverting the transfer functions of analogue integrators [5–7]. The concept can be extended to digital differentiators. The new approach can be broken down into the following four steps:

(*a*) obtain or design an integrator that has the same range and accuracy as the desired differentiator

(*b*) invert the transfer function of the integrator obtained in (*a*)

(*c*) stabilise the transfer function obtained in (*b*) by reflecting the poles that lie outside the unit circle to inside the unit circle

(*d*) compensate the magnitude appropriately by noting that if a pole that lies at a radius $r$ is replaced by a pole that lies at a radius of $1/r$, the magnitude of the resulting transfer function will be multiplied by $r$; thus to compensate for the resulting change in magnitude, the resulting transfer function should be multiplied by $1/r$ [8].

In this Letter, as an example, a new differentiator is obtained by inverting the transfer functions of the Tick integrator [9]. The procedure had been tested successfully on Simpson and other integrators. Tick designed a transfer function that is as close to unity as possible throughout the lower half of the Nyquist interval while still involving only three consecutive terms. In a sense, the Tick integrator is an optimised Simpson integrator. The Tick integrator has two real poles located at $z = +1$ and $z = -1$ and has high accuracy at low frequencies. Thus, the inverse of the transfer function of the Tick integrator results in a numerator which represents a linear phase FIR filter.

In the remainder of the Letter, the Nyquist frequency is normalised to 1. Note that other terms used for the Nyquist frequency are the Nyquist limit, full band, and the foldover frequency, and they all refer to half the sampling frequency.

*Proposed differentiator:* The Tick integrator approximates the ideal integrator up to about half the Nyquist frequency [6]. Its transfer function is

$$G(z) = \frac{T(0{\cdot}3585z^2 + 1{\cdot}2832z + 0{\cdot}3584)}{(z^2 - 1)} \qquad (1)$$

The Tick integrator has two real poles located at $z = +1$ and $z = -1$. It also has two real zeros located at $z = -0{\cdot}30534$ and $z = -3{\cdot}2750$.

In taking the inverse of eqn. 1, a pole that lies outside the unit circle at $z = -3{\cdot}2750$ is obtained. Substituting for the unstable pole a pole at $z = -1/3{\cdot}2750 = -0{\cdot}30534$, the following transfer function is obtained, where $A$ is a gain parameter to be determined below.

$$H(z) = A\frac{(z^2 - 1)}{z^2 + 0{\cdot}611z + 0{\cdot}0932} \qquad (2)$$

Thus, the new differentiator has two real zeros located at $z = +1$ and $z = -1$. It also has a double pole located at $z = -0{\cdot}30534$. Note that the numerator of eqn. 2 represents a linear phase FIR filter with an odd length and an odd symmetry [10]. Thus eqn. 2 may be considered as a linear phase FIR filter, represented by the numerator, in cascade with an IIR filter, represented by the denominator of eqn. 2. Note that the numerator of eqn. 2 is the same, except for a gain factor, as the transfer function for the three-point central difference differentiator [4].

The gain factor that results from inverting eqn. 1 would be $1/0{\cdot}3584T$. With $T = 1$, and compensating for the inversion of the unstable pole, by multiplying by the factor $1/3{\cdot}275$, it would have the value $1/(0{\cdot}3584) \times (3{\cdot}275) = 1/1{\cdot}17376 = 0{\cdot}852$. This is the value that will be used for $A$ in the rest of the paper. Note that the exact value of the gain factor is not critical provided that it is taken into consideration when computing the error difference from the ideal response. Figs. 1 and 2 show the magnitude and phase of the new differentiator, respectively. It is seen that the new differentiator approximates the magnitude of the ideal differentiator up to 0·5 of fullband. In addition, the phase is almost linear in that range. Fig. 3 shows that the error of the magnitude of the new differentiator is less than 1% in the range up to 0·5 of fullband. The new differentiator clearly outperforms the two-point difference differentiator and the three-point central difference differentiator [4]. The proposed differentiator also compares favourably with the state-of-the-art differentiators of Kumar and Dutta-Roy [11]. All the figures in this paper were obtained by using MATLAB* together with the Signal Processing Toolbox.*

*Conclusion:* A new approach for designing differentiators is introduced. The approach consists in inverting the transfer functions of integrators and then stabilising them. As an example, a novel second-order recursive digital differentiator is presented. The low order of the differentiator makes it suitable for real-time applications. It approximates an ideal differentiator in the pass-band region with an accuracy and range comparable to those obtained by higher order filters. In addition, it has an almost linear phase in the pass-band region.

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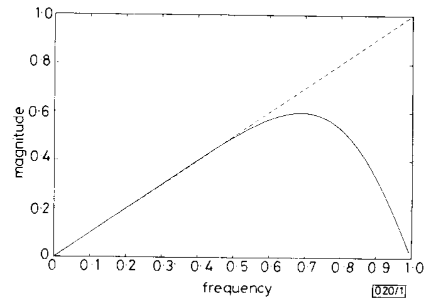


**Fig. 1** *Amplitude response of new differentiator and ideal differentiator*
——— new differentiator
- - - - ideal differentiator

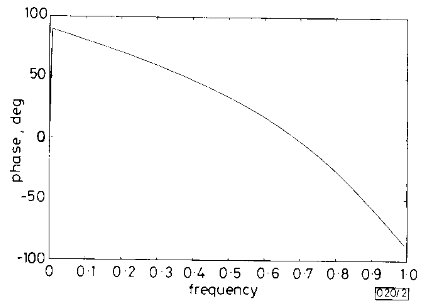


**Fig. 2** *Phase response of new differentiator*

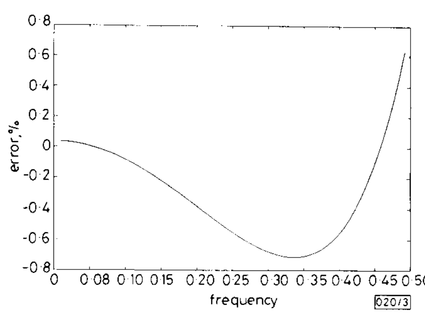


**Fig. 3** *Error of amplitude response of new differentiator*

*1st June 1992*

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# REDUCING $V_{BE}$ WAFER SPREAD OF BIPOLAR TRANSISTOR VIA A COMPENSATION CIRCUIT


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*Indexing terms: Measurement, Integrated circuits, Circuit theory and design*



A circuit which reduces the $V_{BE}$ wafer spread of a standard bipolar transistor in linear ICs is described. This compensation circuit takes advantage of the close correlation between $I_s$ and $\beta r$. The spread of $V_{BE}$ is the major source of output error in IC temperature sensors with intrinsic reference, which thereby require resistive trimming.


Integrated Celsius temperature sensors with an intrinsic reference were introduced commercially [1] in 1984. The basic principle of a temperature sensor with an intrinsic reference [2] is the comparison of a Kelvin voltage $V_{PTAT}$ with the $V_{BE}$ of a transistor as is shown in Fig. 1 and eqn. 1.

$$V_0 = V_{BE7} - V_{PTAT}(R_1/R_2) \tag{1}$$

A small relative variation within the wafer of these terms, at a given temperature, can produce an output error of several

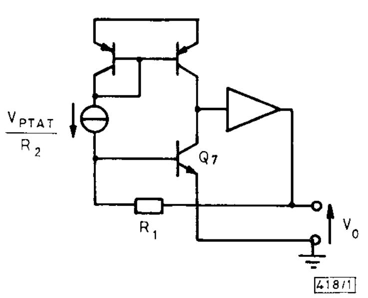


**Fig. 1** *Temperature sensor with intrinsic reference*

degrees; e.g. a spread of $\pm 5°C$ has been measured within a sensor wafer [2] before resistive trimming. The random variation within the wafer of $V_{BE}$, $V_{PTAT}$ and $R_1/R_2$ makes it necessary to perform resistive trimming [1] in every sensor chip at wafer level.

The purpose of this Letter is to describe a compensation circuit that reduces almost to a half the spread of $V_{BE}$, which is the major source of error in eqn. 1. This circuit can be useful in designing a Celsius integrated sensor without resistive trimming.

*Spread of $R_1/R_2$, $V_{PTAT}$ and $V_{BE7}$:* The spread within the wafer of $R_1/R_2$ for a ratio less than 8 : 1 and layout width greater than $40\,\mu m$ using ion implanted resistors can achieve [3] a relative value less than 0·3%.

The spread within the wafer of the Kelvin voltage $V_{PTAT}$ can be reduced by increasing the emitter areas and also using crossconnected transistor quads [2] with centroid [4] layout. Using data [2] for a transistor quad with $6000\,\mu m^2$ emitter area, a spread of $V_{PTAT}$ less than 0·8% can be calculated.

The spread within the wafer of $V_{BE}$ is due [2] to the spread of $I_s$. The value of $V_{BE}$ depends on $I_s$ through the following expression [2]:

$$I_c = I_s \exp(qV_{BE}/kT) \tag{2}$$

Using eqn. 2 and the Dutton histogram [5] for $I_s$ a spread of 2% within the wafer can be calculated for $V_{BE}$. Therefore $V_{BE}$ has the greatest spread of the three parameters in eqn. 1 and can be considered the major source of sensor output error.

A compensation circuit, that reduces the spread of $V_{BE}$ to a half, based on the close correlation [5] between $I_s$ and reverse beta $\beta_r$ in a transistor will be shown.

*Correlation of $I_s$ and $\beta_r$: parameter sensitivity:* Dutton has shown [5] for a standard bipolar transistor wafer that $I_s$ and $\beta_r$ have a good correlation factor of +0·9 and follow the linear regression expression

$$\beta_r = 0{\cdot}19 I_s + 1{\cdot}2 \tag{3}$$

Sensitivity can be defined [6] as

$$S_x^F = \frac{\Delta F/F}{\Delta x/x} \tag{4}$$

or

$$S_x^F = \frac{\partial F}{\partial x} X \tag{5}$$

where $F$ is the output or dependent variable and $x$ is one of the circuit parameters or independent variables.

*Compensation circuit:* The compensation circuit shown in Fig. 2 (patent pending) reduces the spread of $V_{BE}$ considerably.

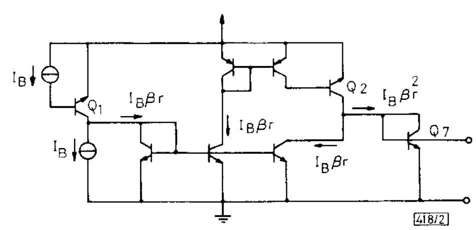


**Fig. 2** *Compensation circuit for reducing spread of $V_{BE7}$*

According to Dutton [5], $I_s$ and $\beta_r$ change within the wafer in the same direction, with good correlation. In the compensation circuit the variation in $V_{BE7}$ due to variations in $I_{s7}$ is significantly reduced. It can be seen that if $I_{s7}$ increases for a given $I_c$ then $V_{BE7}$ decreases according to eqn. 2 in transistor $Q_7$ of Fig. 2; however, as $\beta_r$ increases in the circuit of Fig. 2, the collector current of $Q_7$ increases, and $V_{BE7}$ tends to increase according to eqn. 2, thus compensating for the initial decrease due to $I_{s7}$. In other words $V_{BE7}$ tends to increase according to eqn. 2, thus compensating for the initial decrease due to $I_{s7}$. In other words $V_{BE7}$ of $Q_7$ tends to remain constant.

Simulation of the compensation circuit with PSPICE shows that $V_{BE7}$ is practically insensitive to all parameters except $I_{s7}$ of $Q_7$ and $\beta_r$ of $Q_1$ and $Q_2$ which are both connected in the reverse mode. Thus the variation of $V_{BE7}$ due to these two parameters is as follows:

$$\Delta V_{BE7} \simeq S_{\beta_r}^{V_{BE7}} \frac{\Delta \beta_r}{\beta_r} + S_{I_s}^{V_{BE7}} \frac{\Delta I_s}{I_s} \tag{6}$$

It can be shown from the linear regression expression (eqn. 3)