

The U (used) field denotes whether the corresponding entry in the CARF is empty ($U = 0$) or not ($U = 1$). As soon as an entry is allocated by a register, the U value of the corresponding entry becomes 1. If none of the U -values in the CARF is 0, any further instruction fetches are blocked. When multiple instances with the same register index exist in the CARF, only the L (latest)-value of the most recently registered entry becomes 1, while those of other entries with the same register index become 0. Data dependency and anti-dependency between these registers can be resolved using the L -values.

Instructions fetched from the predicted path of a conditional branch instruction are also registered in the CARF, and the dependency relation among register variables in the CARF can be changed by these instructions. The PL (previous latest) field is used for prompt recovery of the contents of the CARF when branch misprediction has occurred. When the first instruction from the predicted path of a branch instruction has reached the decode unit, each L field is copied into the corresponding PL field. In other words, PL -values preserve the dependency relation among register variables in the CARF before the conditional branch instruction. When misprediction occurs at a branch instruction, the CARF can be returned to the state before the branch instruction only by copying PL to L . This recovery scheme from misprediction requires only bit manipulation between L and PL on the CARF and, therefore, is very fast.

In-order buffer (IB) and exception recovery scheme: When an instruction reaches the decode unit, its destination register is registered into the CARF. If there exists in the CARF an entry (or entries) which has the same destination register as the instruction at the decode unit, the A (address) value of the entry with $L = 1$ is registered in the PA (previous address) field of the tail entry in the IB. The PA of an instruction I , therefore, denotes the address in the CARF of the latest instruction having the same destination register as the instruction I . Therefore, if an instruction I is completed in an in-order sequence, the instruction in the CARF corresponding to the PA of instruction I is past its lifetime and, thus, removed from the CARF by resetting the U -value. When an instruction reaches the decode unit, the PC (program counter), A and PA of the instruction are registered in the tail entry of the IB, and the tail pointer is incremented. If an exception occurs during the operation of the instruction, the E -value of the entry in the IB becomes one.

If an instruction in the head entry has been completed without an exception, the CARF entry corresponding to the PA in the head entry is eliminated from the CARF, and the head pointer is incremented. As a result, instructions included in the current state always exist between the head and the tail pointer of the IB. When an exception is detected during the execution of the instruction at the head of the IB, the following sequence recovers the CARF to the consistent state for precise exception:

(i) *Step 1:* Delete all entries in the CARF having A -values between head and tail-1 of the IB, by resetting the corresponding U -values to 0.

(ii) *Step 2:* Set to 1 the L -value of the entry in the CARF corresponding to PA fields between the head and tail-1 of the IB. By this step, the dependency relation between the registers registered in the CARF before the occurrence of exception due to the instruction at the head entry of the IB can be recovered to the consistent state.

Experimental results and conclusion: An instruction set simulator (ISS) for a data flow architecture supporting out-of-order execution was developed to verify the operation of the proposed architecture using several benchmarks including 24 Lawrence Livermore loops and recursive programs (quick sorting etc.). The data flow architecture consists of three functional units, and each functional unit has a reservation [1] station for out-of-order execution. The CARF with 32 entries in the ISS has shown the maximal instruction-level parallelism for the benchmarks.

Previous solutions [2, 3] for precise exception handling of an out-of-order execution model require separate storage spaces for each state (or backup space for register file contents), which requires complex datapath and hardware resources for exception

recovery. The salient feature of the scheme proposed in this Letter is that the current state and the consistent state are included in a single space called the CARF, which enables prompt and precise exception handling with minimal hardware.

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Design of FIR first order digital differentiators of variable fractional sample delay using maximally flat error criterion

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Indexing terms: Digital filters, Differentiating circuits

Optimum (in a maximally flat frequency response error sense) FIR digital differentiators of variable fractional sample delay are derived that calculate the derivative of an input uniformly sampled discrete-time signal with arbitrary centre frequency at an arbitrarily chosen instant of time within each sampling interval. The proposed class of differentiators includes maximally linear differentiators for low frequencies.

Introduction: In numerous digital signal processing applications, especially in space navigation and robotics, the precise values of differentiation of an available uniformly sampled waveform, performed in a frequency band around a given angular frequency θ and at an optional instant of time, thus provided with, generally, a noninteger delay τ with respect to the sampling instants of the input data, are required. This Letter proposes an efficient one-stage FIR digital differentiator with variable fractional sample delay (DDVFSD) design capable of calculating the derivative and delaying the input waveform simultaneously with very low relative errors in the frequency response around a given centre frequency.

Design: The frequency response of an ideal DDVFSD is given by

$$D_{\tau}(\omega) \triangleq j\omega \exp(-j\omega\tau) \quad (1)$$

where τ stands for an optional, generally noninteger, time delay, $j \triangleq \sqrt{-1}$ and ω is the normalised angular frequency. An FIR approximation $D_{\tau\theta}(\omega)$, of $D_{\tau}(\omega)$, around some angular frequency $\theta \in \langle -\pi, \pi \rangle$, may be written as

$$D_{\tau\theta}(\omega) \triangleq \sum_{n=0}^{N-1} d_{\tau\theta}(n) \exp(-j\omega n) \quad -\pi + \theta \leq \omega < \pi + \theta \quad (2)$$

where $d_{\tau\theta}(n)$, $n = 0, 1, \dots, N-1$, is the DDVFSD filter impulse response of length N .

Maximal flatness of the DDVFSD frequency response approximation error

$$E_{\tau\theta}(\omega) \triangleq D_{\tau}(\omega) - D_{\tau\theta}(\omega) \quad (3)$$

at given $\omega = \theta$ demands that

$$d^i [E_{\tau\theta}(\omega)] / d\omega^i = 0 \quad \omega = \theta \quad i = 0, 1, \dots, N-1 \quad (4)$$

Forcing the conditions of eqn. 4 gives the following general solution for the DDVFSD coefficients:

$$d_{\tau\theta} = Q_{\theta}^{-1} \mathcal{I}_{\theta} \quad (5)$$

where

$$\underline{d}_{\tau\theta} \triangleq [d_{\tau\theta}(0), d_{\tau\theta}(1), \dots, d_{\tau\theta}(N-1)]' \quad (6)$$

Q_θ is the $N \times N$ Vandermonde matrix whose entries are

$$q_{ik} \triangleq (k-1)^{i-1} \exp[-j(k-1)\theta] \quad i, k = 1, 2, \dots, N \quad (7)$$

and

$$\underline{\mathcal{L}}_\theta \triangleq \exp(-j\theta\tau) \times [j\theta, j\theta\tau-1, \tau(j\theta\tau-2), \dots, \tau^{N-2}(j\theta\tau-(N-1))]' \quad (8)$$

where ' stands for transposition.

We now proceed to obtain an explicit formula for the DDVFS coefficients, $d_\theta(n)$. This can be done effectively by using the Cramer rule to solve eqn. 5. In doing so, we obtain for $n = 0, 1, \dots, N-1$

$$d_{\tau\theta}(n) = \frac{j\theta \prod_{\substack{k=0 \\ k \neq n}}^{N-1} (\tau-k) - \sum_{\substack{l=0 \\ l \neq n}}^{N-1} \prod_{\substack{k=0 \\ k \neq l, n}}^{N-1} (\tau-k)}{\prod_{\substack{k=0 \\ k \neq n}}^{N-1} (n-k)} \exp[j\theta(n-\tau)] \quad (9)$$

The first term in eqn. 9 can be recognised as the formula for the coefficients of a maximally flat tunable FIR delayer, multiplied by $j\theta$ (see eqn. 7 in [1]).

It is worth noting that a causal FIR filter of length N introduces a transport delay of $\bar{\tau} \triangleq (N-1)/2$ sampling intervals. Hence, it is convenient to express the variable delay τ as $\tau = \bar{\tau} + \epsilon$, where ϵ is the true fractional sample delay introduced by the DDVFS. For practical reasons it is preferable to use $\tau \in \langle N/2 - 1, N/2 \rangle$, thus $\epsilon \in \langle -1/2, 1/2 \rangle$, because for such τ and N , θ fixed, the bandwidth of good approximation is the widest.

In the lowpass case, i.e. when $\theta = 0$, and for $\tau = \bar{\tau}$ fixed, the coefficients of eqn. 9 simplify to the following:

$$d_{\tau 0}(n) = \frac{-\sum_{\substack{l=0 \\ l \neq n}}^{N-1} \prod_{\substack{k=0 \\ k \neq l, n}}^{N-1} (N-2k-1)}{2 \prod_{\substack{k=0 \\ k \neq n}}^{N-1} (n-k)} \quad n = 0, 1, \dots, N-1 \quad (10)$$

It can be shown that for this particular case and for N odd, the coefficients of the DDVFS in eqn. 10 are equal to the respective coefficients of maximally linear FIR digital differentiators derived by Kumar and Dutta Roy for low frequencies [2], as given by

$$d_{\tau 0}(n) = \begin{cases} d_{n+1}/2 & n = 0, 1, \dots, (N-1)/2 - 1 \\ 0 & n = (N-1)/2 \\ -d_{N-n}/2 & n = (N+1)/2, \dots, N-1 \end{cases} \quad (11)$$

where d_k , $k = 1, 2, \dots, (N-1)/2$, are the coefficients given by eqn. 8 or 14 in [2]. That is because for $\tau = \bar{\tau}$, $\theta = 0$, the maximally flat frequency response approximation error criterion is equivalent to the criterion of maximal linearity of the DDVFS frequency response. Thus, the DDVFS derived herein is a generalisation of the digital differentiator design suggested in [2], for arbitrary N , τ and θ .

Performance: Fig. 1 shows the magnitude response, the group delay response and the relative error (RE) of approximation curves over the entire band of frequencies $\omega \in \langle -\pi, \pi \rangle$ for the proposed DDVFS of length $N = 10$ for selected ϵ , thus also τ , and θ . The RE of the frequency response approximation is defined as

$$RE(\omega) \triangleq |E_{\tau\theta}(\omega)/D_{\tau\theta}(\omega)| \quad (12)$$

As expected, extremely low relative errors are available in the frequency band centred around $\omega = \theta$ with attractively low order of FIR filter structure. For example, for θ and ϵ as in Fig. 1, frequency response accuracy better than 99.999% ($RE < -100$ dB) can be achieved over the band of 0.39π width with an order $N-1 = 9$ of the structure.

Conclusions: Efficient FIR digital differentiators of variable fractional sample delay, suitable for operation around any centre frequency with very low relative errors in the frequency response,

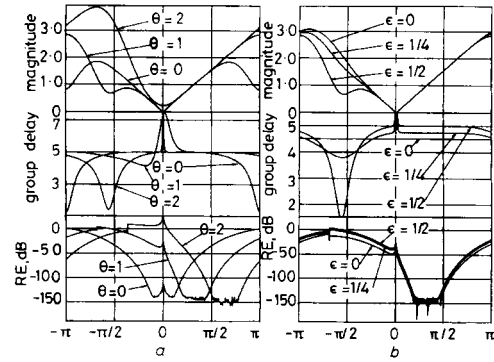


Fig. 1 Magnitude response $|D_{\tau\theta}(\omega)|$, group delay response $-dD_{\tau\theta}(\omega)/d\omega$, and frequency response relative error $RE(\omega)$, of proposed DDVFSs for $N = 10$

a $\epsilon = 0.5$ ($\tau = 5.0$), $\theta = 0, 1$ and 2 rad
b $\theta = 1$ rad, $\epsilon = 0, 1/4$ and $1/2$ ($\tau = 4.5, 4.75$ and 5.0)

have been proposed. A mathematical formula for calculation of the exact values of the coefficients needed in the design has been derived. A useful relation between the coefficients of the proposed DDVFSs and the coefficients of their subclass, namely, of digital differentiators for low frequencies [2], has also been pointed out.

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Two port adaptor for wave digital filters based on nonredundant radix-4 arithmetic

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Indexing terms: Wave digital filters, Filters

Wave digital filters synthesised from two port adaptors are highly recursive structures and hence for high speed implementations it is essential to reduce the latency of the adaptor. This is directly related to the number of addition levels used. Nonredundant radix-4 arithmetic has already been shown to nearly halve the number of levels compared with an un-coded multiplication with much less hardware overhead than the modified Booth algorithm. In the Letter, nonredundant radix-4 arithmetic is applied to the two-port adaptor. The results compare favourably with previous approaches for most coefficient wordlengths of practical interest.

Introduction: Wave digital filters (WDFs) are important IIR filter forms with many desirable properties from a filter design aspect [1]. When constructed from two port adaptors they offer simplicity and modularity that makes them attractive for VLSI implementation. However, to exploit WDFs in high speed applications, problems associated with their intrinsic tightly recursive structure must be solved. Fig. 1 shows the typical structure encountered. The two port adaptors realise the following arithmetic: