dielectric constant close to unity. A U-slot is cut into the patch. The patch is proximity fed by an L-shaped coaxial probe, and it is excited in the TM_{11} mode. The patch has the following parameters: \( C_d = 34\text{ mm}, L_d = 15\text{ mm}, L_{st} = 5.5\text{ mm}, U^0 = 12\text{ mm}, U^0_c = 20\text{ mm}, a = 4\text{ mm}, b = 6\text{ mm}, c = 2\text{ mm}, D = 3\text{ mm}, R = 0.5\text{ mm} \) and \( H = 9\text{ mm} \) (<0.1\( \lambda_o \), where \( \lambda_o \) is the free-space wavelength corresponding to the centre frequency, 3.6 GHz, of the patch antenna).

Fig. 2 SWR and gain against frequency

Measured results and discussion: The SWR and gain of the antenna are shown in Fig. 2. The SWR is \( \leq 2 \) in the frequency range 2.94-4.31 GHz, corresponding to an impedance bandwidth of 38% centred at 3.6 GHz. The measured gain in the broadside direction is \( \geq 6\text{ dB} \) over the majority of the band. Fig. 3 shows the input impedance. The bandwidth enhancement arises from three sources: (i) the relatively thick substrate, (ii) the introduction of a capacitance in parallel with the patch due to the U-slot, and (iii) the introduction of a capacitance in series with the patch due to the L-probe. Thus, the inductance introduced by the vertical arm \( (L_s) \) of the L-probe due to the thick substrate can be partly suppressed by the capacitance.

Fig. 3 Input impedance against frequency

Conclusions: We have described the combination of the L-probe and U-slot broadening techniques, in the design of a broadband single-layer circular patch antenna. For a foam substrate of thickness 0.1\( \lambda_o \), the bandwidth of the resulting antenna was 15% wider than that using the U-slot alone and 14% wider than that using the L-probe alone.

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References


Compact formulas for least-squares design of digital differentiators

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New compact and simple formulas for the design of digital differentiators based on the least squares method are proposed. The new expressions allow a very fast and precise computation of the filter coefficients. Furthermore, using the proposed analytical solution, the need to solve the system of linear equations for the case of fullband differentiators is avoided.

Introduction: Digital differentiators (DDs) are extensively used in a large number of practical applications, including radar and sonar systems, speech processing systems, modulation schemes, etc. They are generally designed using the minimax criterion [1], the least squares method [2], the Fourier series, etc. The eigenfilter method [3, 4] can be efficiently used for first and higher-order
DDs. Other algorithms and expressions are given in [5, 6] for calculating the weighting coefficients of maximally linear FIR differentiators.

This Letter presents the derivation of new formulas for the least squares design of DDs. Two different cases, fullband and non-fullband differentiators, are considered. This technique results in a lower computational complexity than the minimax and eigenfilter methods.

\[Q = \int_0^{\pi} e(\omega)e^T(\omega) d\omega \quad d = \int_0^{\pi} D(\omega)e(\omega) d\omega\]

**Fig. 2** Error curves for fullband case 4 differentiator with length N = 76

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**Proposed formulas**

\[d(n) = \begin{cases} 2\pi \frac{\sin(n-1/2)\omega_p - \cos(n-1/2)\omega_p}{2\pi(2n-1)\omega_p} & n \text{ odd} \\ \frac{2\pi \sin(n-1/2)\omega_p}{2\pi(2n-1)\omega_p} & n \text{ even} \end{cases}\]

where \(\sin x = \sin x \times x\). The elements of the matrix \(Q\) are derived as follows:

\[q(n, m) = \begin{cases} \frac{2\pi \sin(n-m)\omega_p - \sin(n+m-1)\omega_p}{2\pi(2n-1)\omega_p} & n \neq m \\ \frac{\sin(n-l)\omega_p}{2\pi(2n-1)\omega_p} & l = 0 \text{ for } 1 \leq n, m \leq \frac{N-1}{2} \\ 0 & n = m \end{cases}\]

For the case of the fullband DD (\(\omega_0 = \pi\), only when \(N\) is even) we obtain very simple and compact formulas for the entries of \(d\) and \(Q\):

\[d(n) = \begin{cases} 4\pi(-1)^{n-1} & 1 \leq n \leq \frac{N}{2} \end{cases}\]

and

\[q(n, m) = \begin{cases} \frac{\sin(n-m)\omega_p}{2\pi(2n-1)\omega_p} & n \neq m \\ 0 & n = m \end{cases}\]

Finally, we find an exact formula for the vector \(b\) from eqn. 2:

\[b(n) = \frac{8\pi(-1)^{n-1}}{2\pi(2n-1)\omega_p} \sin(n-1/2)\omega_p \quad \text{N even}\]

and so avoid solving the system of linear equations. Consequently, the amplitude response of the fullband DD designed by the least squares method can be calculated directly as

\[M(\omega) = \frac{2\pi}{\pi} \sum_{n=1}^{N/2} (-1)^{n+1} \sin(n-1/2)\omega_p \quad \text{N even}\]

**Examples and conclusions:** A MatLab based source was developed to demonstrate the flexibility and effectiveness of the new relations. Fig. 1 shows plots of the amplitude responses of non-fullband and fullband differentiators with different lengths \(N\). The error function \(E = D(\omega) - M(\omega)\) against frequency is given in Fig. 2 (for the proposed method and the minimax method). A better error function for the fullband DD was obtained with the new formulas in most of the frequency band, except in the narrowband region near the cutoff edge. The error function for the non-fullband case is close to that for the minimax method. As a
result, very low errors are achieved (for example, there is a peak error of 0.801 x 10^-5 or -142 dB for DD with N = 41, a0 = 0.75%).

References


Current division circuit implemented using CMOS technology

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A simple circuit is proposed for dividing one current by another. This circuit is composed of two MOS transistors, a voltage comparator, and two capacitors. The divider operates well at low currents. Using 1.5μm single-poly CMOS technology, the proposed circuit occupies a silicon area of ~30μm x 40μm.

Introduction: As the voltage signal swing in integrated circuits decreases with shrinking transistor feature size, current-mode signal processing is becoming an attractive alternative to voltage-mode signal processing [1]. In the design and implementation of CMOS circuits for current-mode arithmetic operations, the processing accuracy is a challenging issue. Current division can be achieved using MOS transistor characteristics [2], but the accuracy is limited by the device mismatch at low currents. A simple current divider is proposed in this Letter in which device matching is not required. Consequently, this circuit will operate at low currents to achieve low-power operation.

Circuit description: The schematic diagram of the proposed current divider is shown in Fig. 1. The circuit consists of two MOS transistors, two capacitors, and a voltage comparator. The two input currents, i1 and i2, are the denominator and numerator, respectively. The output signal is voltage VC2. A pulse signal 'reset' with a narrow pulselwidth TR is used to initialise the circuit operation. The frequency of the reset signal is determined according to the dynamic range of the input currents. The circuit operates as follows: when the reset is set at the high level, VC2 is set to 0 V. The voltage comparator output Vp is thus set to 0 V forcing M2 off. At this instant (i.e. the beginning of the reset pulse) VC2 begins to rise due to i1, however, VC2 remains at 0 V for the duration of TR. The reset pulse returns to 0 V, after a time TR, at which point VC2 begins to rise due to the charging of C1 via i2. When VC1 reaches the comparator threshold voltage Vth, Vp is switched to the high level enabling the charging process for C2. The comparator output Vp will remain at the low level for a time duration TR. The actual charging time for capacitor C1 is TR - TR = Vth/C1. The end of the charging process, the output voltage is given by

\[ V_{C2} = V_{th} + \frac{i_1}{C_1} \left( C_1 + C_2 \right) \]

where \( C_1 = C_{C1} / C_2 \) and \( \Delta V_{C2} = V_{th} / C_2 \). Provided that \( TR << T_R \), \( \Delta V_{C2} \) may be neglected so that \( V_{C2} = \frac{i_1}{C_2} \), thus realising the current division. Because \( \Delta V_{C2} \) is independent of transistor parameters, the operation accuracy is insensitive to transistor parameters, thus allowing the proposed current divider to operate at very low currents.

Simulation results: The circuit in Fig. 1 has been simulated using HSPICE with the transistor models of 1.5μm CMOS technology. Fig. 2 shows the variation of the output voltage VC2 against the numerator current i1 for different values of the denominator currents i2.

![Fig. 1: Schematic circuit diagram and signal waveforms of proposed current divider](image)

Duration TR is inversely proportional to current i1 and value of VC2 at end of TR is proportional to current ratio i1/i2.

![Fig. 2: Simulation results for output voltage VC2 against numerator current i1 in proposed current divider using constant denominator currents i2](image)

The accuracy of the divider circuit is primarily limited by the finite reset pulselwidth TR. This is demonstrated by plotting the output voltage VC2 against the ratio i1/i2 for two different denominator currents, as shown in Fig. 3.

As mentioned previously, a discrepancy exists in the output voltage and this is given by \( \Delta V_{C2} = V_{th} / C_2 \). Hence, \( \Delta V_{C2} \) will be greater for larger values of i0. Despite this, the deviation observed in Fig. 3 is <1.5% for current ratios (i1/i2) below 1.6.

Applications: The current divider circuit of Fig. 1 may be used in analogue signal processing systems for division operations. It may also be used for current-to-voltage conversion combined with a normalisation. A significant consequence of the normalisation is that the dynamic range of the input current signal (i1) may be

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